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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,427	06/28/2004	Shuusuke Kantake	HEIWA.014AUS	9332

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MURAMATSU & ASSOCIATES
114 PACIFICA
SUITE 310
IRVINE, CA 92618

EXAMINER	
CHARIOUI, MOHAMED	
ART UNIT	**PAPER NUMBER**
2857	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/500,427	KANTAKE, SHUUSUKE	
	Examiner	Art Unit	
	Mohamed Charioui	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,7-9 and 12* is/are rejected.

7)☒ Claim(s) *2,3,6,10 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 June 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/28/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. **Figure 10** is objected to for the following minor informalities: Applicant refers to Fig. 10 in the specification, pages 2-5. Applicant should label Fig. 10 as prior art.

Claim Objections

2. **Claim 7** is objected to because of the following informalities:

Claim 7 recites the limitation "the timing data output from the encoder" in page 5, line 14. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshiba (U.S. 6,457,148).

Yoshiba teaches a first LSI tester which inputs a first signal output from the LSI to be measured and which acquires the first signal by a plurality of strobes having a certain timing interval to output level data in a time series (see col. 8, lines 10-53; col. 11, lines 1-45; Fig 1; and Fig. 6); a second LSI tester which inputs a second signal

output from the LSI to be measured and which acquires the second signal by a plurality of strobes having a certain timing interval to output level data in a time series (see col. 8, lines 10-53; col. 11, lines 1-45; Fig 1; and Fig. 6); and a selection circuit which is disposed in at least one of the first and second LSI testers and which inputs the level data of the time series output from the first and second LSI testers to select the second signal input into the second LSI tester at a timing of the first signal input into the first LSI tester and which outputs the second signal as the data to be measured of the LSI to be measured (see col. 11, line 1 to col. 12, line 45 and col. 13, lines 11-26).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 5, 7 and 8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshiba in view of Gillis et al. (U.S. 6,058,496).

Yoshiba teaches the system as stated above except for a jitter distribution analysis means for inputting the level data of the time series output from the first LSI tester to acquire a timing of the output signal input into the first LSI tester and for outputting the distribution of the jitters of the output signal.

Gillis et al. teach this feature (see col. 1, lines 13-29 and col. 11, lines 44-61). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Gillis et al.'s teaching into Yoshiba's invention because it

would analyze and eliminate the tester error. Therefore, the test result data would be more accurate and reliable.

5. **Claims 9 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshiba in view of Chu et al. (U.S. 5,384,541).

Yoshiba teaches the system as stated above except for a phase difference detection circuit which is disposed in at least one of the first and second LSI testers and which inputs the level data of the time series output from the first and second LSI testers to calculate a difference between a timing of the first signal input into the first LSI tester and that of the second signal input into the second LSI tester and which outputs the phase difference.

Chu et al. teach this feature (see col. 1, line 65 to col. 2, line 10 and col. 2, lines 40-62). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Chu et al.'s teaching into Yoshiba's invention because it would measure the time delay between the first and the second input signal to determine the phase difference between the two signals. Therefore, accurate and reliable analysis of the test results would be performed.

Allowable Subject Matter

6. **Claims 2, 3, 6, 10 and 11** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claims 2 and 3, none of the prior art of record teaches or suggests that the second LSI tester comprises a second time interpolator including: a sequential

circuit which inputs the output data output from the LSI to be measured; and a delay circuit which successively inputs the strobe delayed at a certain timing interval into the sequential circuit and which allows the sequential circuit to output the level data of the time series, and the selection circuit comprises a selector which selects one data from the level data of the time series input from the second time interpolator using the level data of the time series coded by the first time interpolator as a selection signal to output data to be measured of the LSI to be measured, in combination with the rest of the claim limitations.

Regarding claims 2 and 3, none of the prior art of record teaches or suggests the second LSI tester comprises a second time interpolator including: a sequential circuit which inputs the output data output from the LSI to be measured; a delay circuit which successively inputs the strobe delayed at a certain timing interval into the sequential circuit and which allows the sequential circuit to output the level data of the time series; and an encoder which inputs the level data of the time series output from the sequential circuit and which encodes the level data into timing data indicating an edge timing of the output data of the LSI to be measured to output the timing data, and the phase difference detection circuit comprises: a calculation circuit which subtracts the level data of the time series encoded by the first time interpolator and the level data of the time series encoded by the second time interpolator; and a decoder which decodes a calculation result of the calculation circuit, and the phase difference detector outputs the data decoded by the decoder as a phase difference, in combination with the rest of the claim limitations.

Prior art

7. The prior art made record and not relied upon is considered pertinent to applicant's disclosure:

Miller ['575] discloses cross-correlation timing calibration for wafer-level IC tester interconnect system.

Yamashita ['098] discloses semiconductor test system.

Sato et al. ['579] disclose semiconductor integrated circuit and design method and manufacturing method of the same.

Behrens ['995] discloses apparatus for generating test signals.

Ohtomo ['255] discloses IC tester.

Ochiai et al. ['392] disclose semiconductor test system.

Kobayashi ['334] discloses variable delay element test circuit.

Takagi et al. [096] disclose test board for testing a semiconductor device utilizing first and second delay elements in a signal-transmission-path.

Contact information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohamed Charioui whose telephone number is (571) 272-2213. The examiner can normally be reached Monday through Friday, from 9 am to 6 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S Hoff can be reached on (571) 272-2216. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mohamed Charioui

9/14/05

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800